

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Application-specific gate drive range:
Motor Drive: 12 V to 20 V (AUIRS2127/AUIRS2128)
Automotive: 9 V to 20 V (AUIRS21271/AUIRS21281)
- Undervoltage lockout
- Desaturation Over Current Protection
- 3.3 V, 5 V, and 15 V input logic compatible
- FAULT lead indicates shutdown has occurred
- Output in phase with input (AUIRS2127/AUIRS21271)
- Output out of phase with input (AUIRS2128/AUIRS21281)
- Lead-free, RoHS compliant
- Automotive qualified*

Typical Applications

- Fork Lift motor drives
- hydraulic pumps
- IGBT drive with Desaturation Detection
- General purpose three phase inverters

Product Summary

Topology		Single
V_{OFFSET}		$\leq 600 \text{ V}$
V_{OUT}	AUIRS212(7,8)	12 V – 20 V
	AUIRS212(71,81)	8.4 V – 20 V
$I_{\text{O+}} \& I_{\text{O-}}$ (typical)		290 mA & 600 mA
$t_{\text{ON}} \& t_{\text{OFF}}$ (typical)		200 ns & 175 ns

Package Options



8-Lead SOIC

Typical Connection Diagram

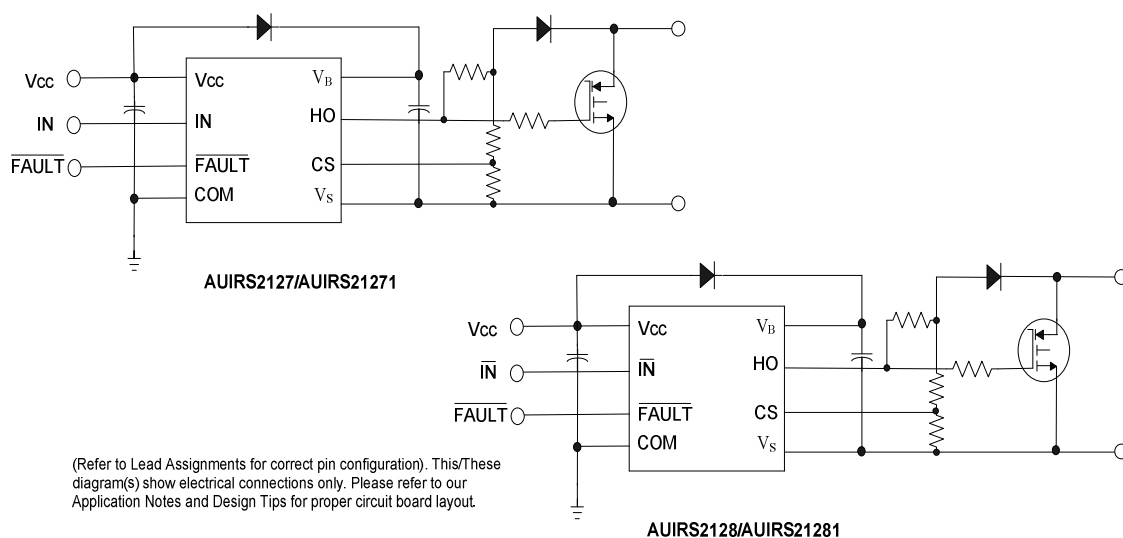


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Description

The AUIRS2127S/AUIRS2128S/AUIRS21271S/AUIRS21281S are high voltage, high speed power MOSFET and IGBT drivers. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs, down to 3.3 V. The protection circuitry detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high- side or low-side configuration which operates up to 600 V.

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q100 ^{††})	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8	MSL3 ^{†††} 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (Pass +/-150V) (per AEC-Q100-003)	
	Human Body Model	Class H1B (Pass +/-1000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A ^{††††} (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

†††† FAULT pin not stressed.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which permanent damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the “Recommended Operating Condition” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	-0.3	625	V
V_S	High-side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High-side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Logic supply voltage	-0.3	25	
V_{IN}	Logic input voltage	-0.3	$V_{CC} + 0.3$	
V_{FLT}	FAULT output voltage	-0.3	$V_{CC} + 0.3$	
V_{CS}	Current sense voltage	$V_S - 0.3$	$V_B + 0.3$	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq 25^\circ\text{C}$	—	0.625	W
R_{thJA}	Thermal resistance, junction to ambient	—	200	$^\circ\text{C}/\text{W}$
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differentials.

Symbol	Definition	Min.	Max.	Units	
V_B	High-side floating supply voltage	(AUIRS2127/AUIRS2128)	$V_S + 12$	$V_S + 20$	V
		(AUIRS21271/AUIRS21281)	$V_S + 9$	$V_S + 20$	
V_S	High-side floating supply offset voltage	†	600		
V_{HO}	High-side floating output voltage	V_S	V_B		
V_{CC}	Logic supply voltage	10	20		
V_{IN}	Logic input voltage	0	V_{CC}		
V_{FLT}	FAULT output voltage	0	V_{CC}		
V_{CS}	Current sense voltage	V_S	$V_S + 5$		
T_A	Ambient temperature	-40	125	$^\circ\text{C}$	

† Logic operational for V_S of -5 to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$.
(Please refer to the Design Tip DT97 -3 for more details).

Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ with bias conditions of $V_{\text{BIAS}} (V_{\text{CC}}, V_{\text{BS}}) = 15\text{ V}$. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to COM. The V_{O} and I_{O} parameters are referenced to V_{S} .

Symbol	Definition		Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	(AUIRS2127/AUIRS21271)	2.5	—	—	V	$V_{\text{CC}} = 10\text{ V to } 20\text{ V}$
	Logic "0" input voltage	(AUIRS2128/AUIRS21281)					
V_{IL}	Logic "0" input voltage	(AUIRS2127/AUIRS21271)	—	—	0.8		
	Logic "1" input voltage	(AUIRS2128/AUIRS21281)					
$V_{\text{CSTH+}}$	CS input positive going threshold	(AUIRS2127/AUIRS2128)	180	250	320	mV	
		(AUIRS21271/AUIRS21281)	1.5	1.8	2.1	V	
V_{OH}	High level output voltage, $V_{\text{BIAS}} - V_{\text{O}}$		—	0.05	0.2	V	$I_{\text{O}} = 2\text{ mA}$
V_{OL}	Low level output voltage, V_{O}		—	0.02	0.1	V	
I_{LK}	Offset supply leakage current		—	—	50	μA	$V_{\text{B}} = V_{\text{S}} = 600\text{ V}$
I_{QBS}	Quiescent V_{BS} supply current		—	300	925		$V_{\text{IN}} = 0\text{ V or } 5\text{ V}$
I_{QCC}	Quiescent V_{CC} supply current		—	60	130		$V_{\text{IN}} = 5\text{ V}$
$I_{\text{IN+}}$	Logic "1" input bias current		—	7.0	15		$V_{\text{IN}} = 0\text{ V}$
$I_{\text{IN-}}$	Logic "0" input bias current		—	—	5.0		$V_{\text{CS}} = 3\text{ V}$
$I_{\text{CS+}}$	"High" CS bias current		—	—	5.0		$V_{\text{CS}} = 0\text{ V}$
$I_{\text{CS-}}$	"High" CS bias current		—	—	5.0		
$V_{\text{BSUV+}}$	V_{BS} supply undervoltage positive going threshold	(AUIRS2127/AUIRS2128)	8.8	10.3	11.8		V
		(AUIRS21271/AUIRS21281)	6.3	7.2	8.2		
$V_{\text{BSUV-}}$	V_{BS} supply undervoltage negative going threshold	(AUIRS2127/AUIRS2128)	7.5	9.0	10.6		
		(AUIRS21271/AUIRS21281)	6.0	6.8	7.7		
$I_{\text{O+}}$	Output high short circuit pulsed current ^(†)		200	290	—	mA	$V_{\text{O}} = 0\text{ V}, V_{\text{IN}} = 5\text{ V}$ $\text{PW} \leq 10\text{ }\mu\text{s}$
$I_{\text{O-}}$	Output low short circuit pulsed current ^(†)		420	600	—		$V_{\text{O}} = 15\text{ V}, V_{\text{IN}} = 0\text{ V}$ $\text{PW} \leq 10\text{ }\mu\text{s}$
$R_{\text{on, FLT}}$	FAULT – low on resistance		—	125	—	Ω	

(†) Guaranteed by design

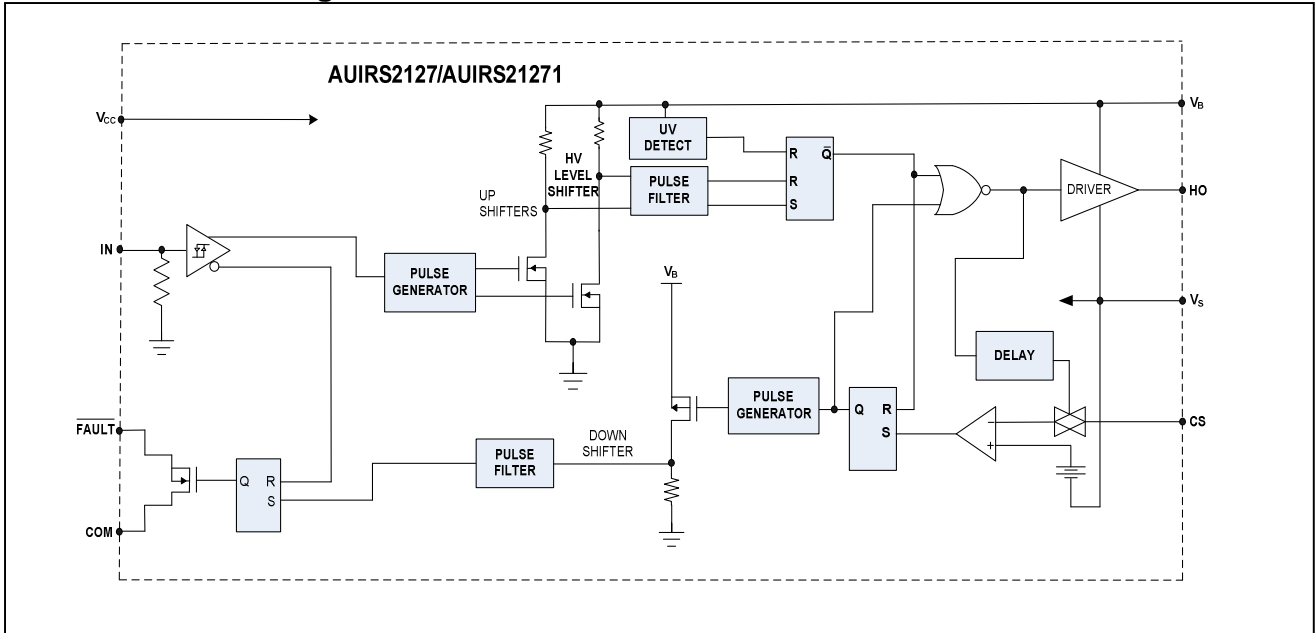
Dynamic Electrical Characteristic

Unless otherwise noted, these specifications apply for an operating junction temperature range of $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ with bias conditions of $V_{\text{BIAS}} (V_{\text{CC}}, V_{\text{BS}}) = 15\text{ V}$, $C_{\text{L}} = 1000\text{ pF}$.

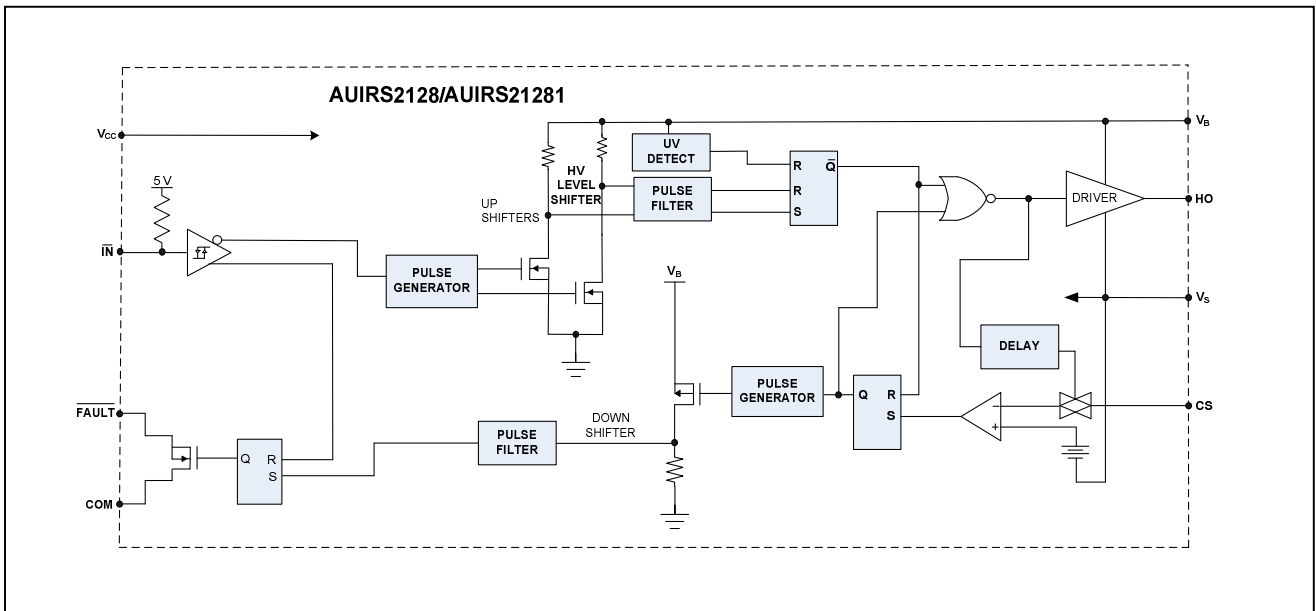
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	200	275	ns	$V_{\text{S}} = 0\text{ V}$
t_{off}	Turn-off propagation delay	—	175	275		$V_{\text{S}} = 600\text{ V}$
t_{r}	Turn-on rise time	—	80	130		
t_{f}	Turn-off fall time	—	40	65		
t_{bl}	Start-up blanking time	475	750	985		
t_{CS}	CS shutdown propagation delay	—	65	360		
t_{fit}	CS to FAULT pull-up propagation delay	—	270	510		

Note: Please refer to figures in Parameter Temperature Trends section

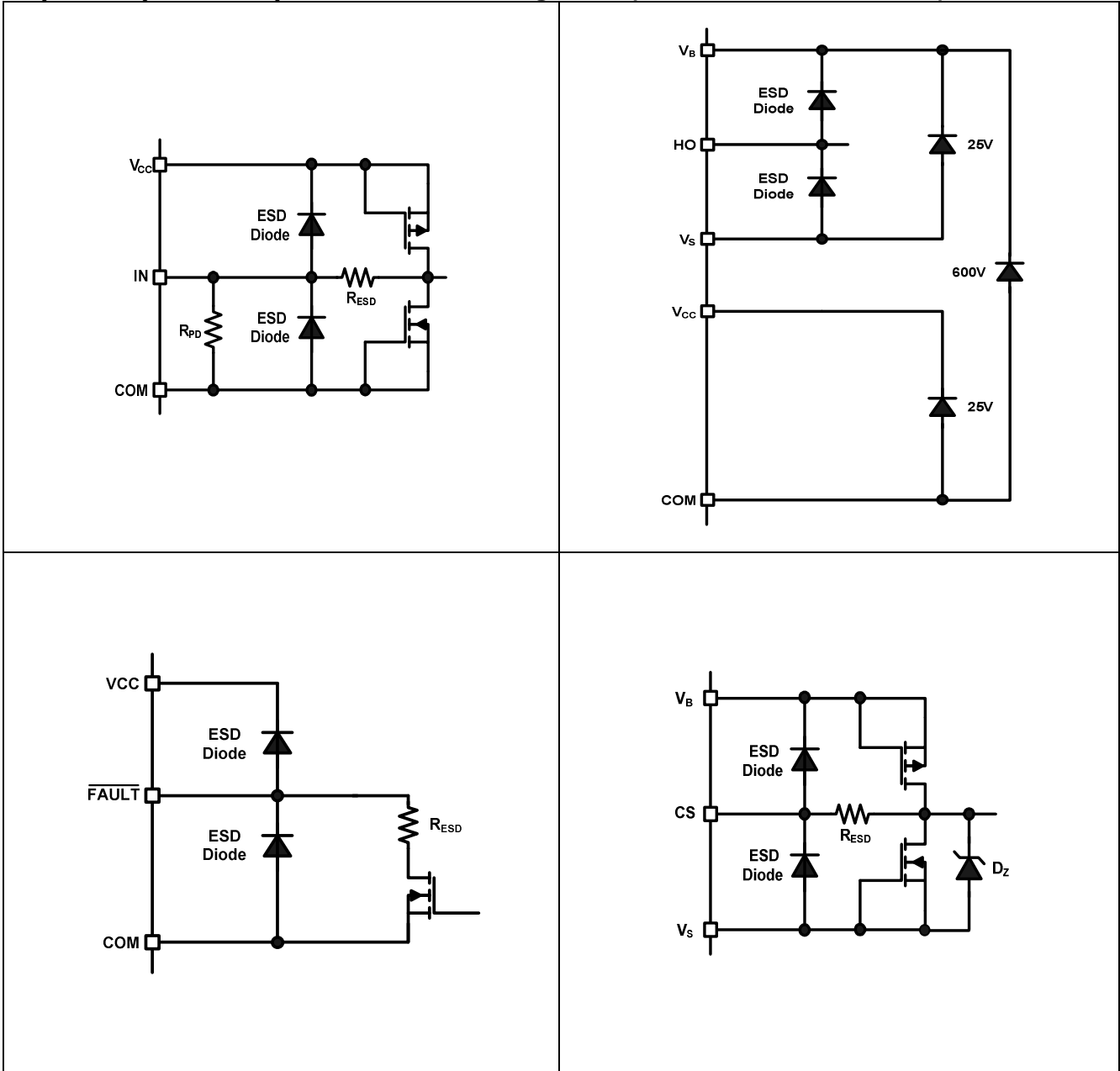
Functional Block Diagram: AUIRS2127/AUIRS21271



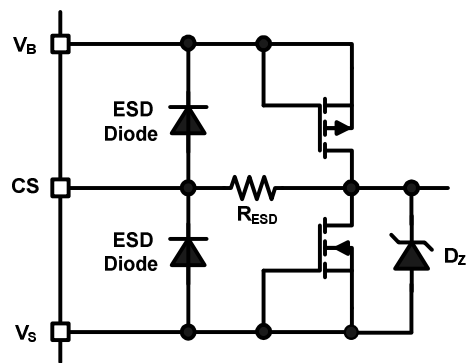
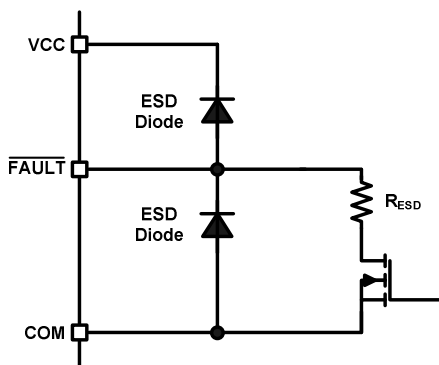
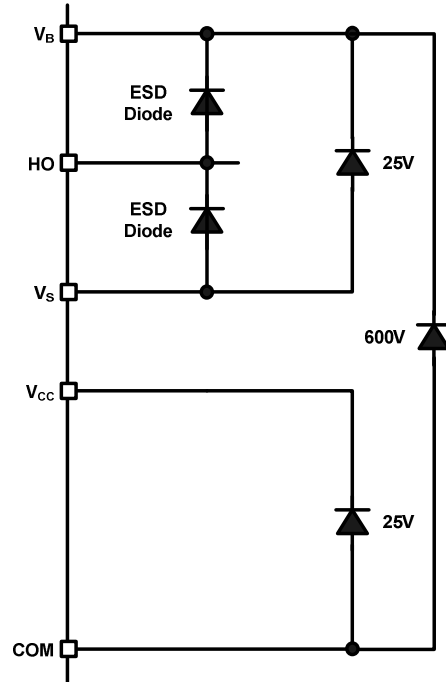
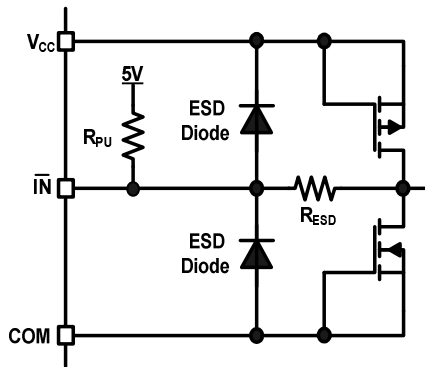
Functional Block Diagram: AUIRS2128/AUIRS21281



Input/Output Pin Equivalent Circuit Diagrams: (AUIRS2127/AUIRS21271)



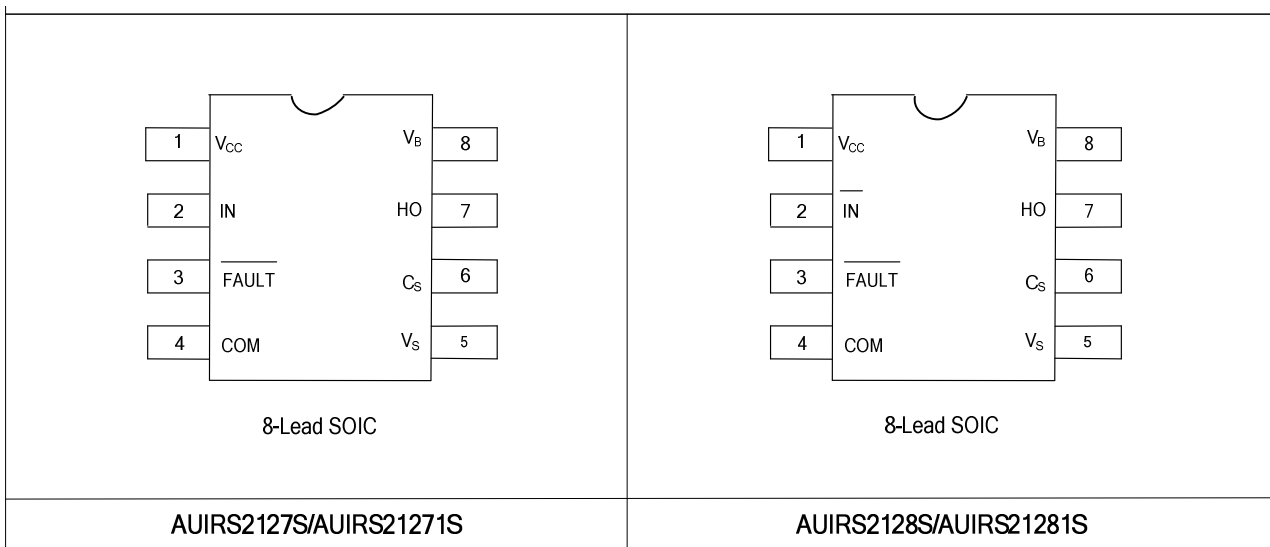
Input/Output Pin Equivalent Circuit Diagrams: (AUIRS2128/AUIRS21281)



Lead Definitions

PIN	Symbol	Description
1	V_{CC}	Low-side and gate drive supply
2	\overline{IN} IN	Logic input for gate driver output (HO), in phase with HO (AUIRS2127/AUIRS21271) Logic input for gate driver output (HO), out of phase with HO (AUIRS2128/AUIRS21281)
3	\overline{FAULT}	Indicates over-current shutdown has occurred, negative logic
4	COM	Logic ground
5	V_S	High-side floating supply return
6	C_S	Current sense input to current sense comparator
7	HO	High-side gate drive output
8	V_B	High-side floating supply

Lead Assignments



Application Information and Additional Details

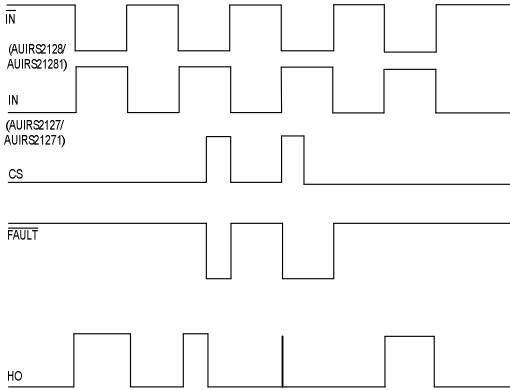


Figure 1: Input/Output Timing Diagram

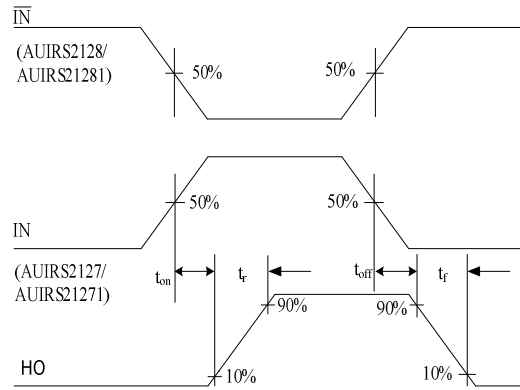


Figure 2: Switching Time Waveform Definition

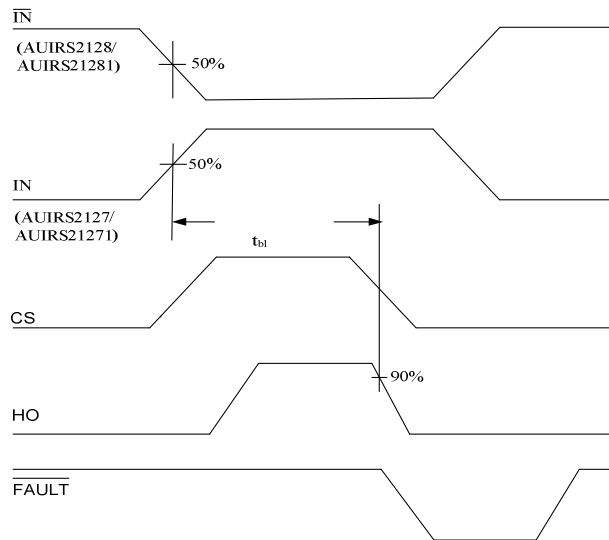


Figure 3: Start-Up Blanking Time Waveform Definitions

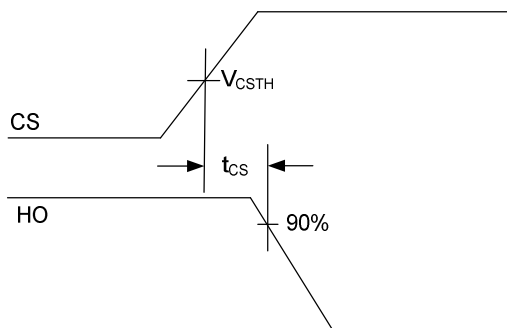


Figure 4: CS Shutdown Waveform Definitions

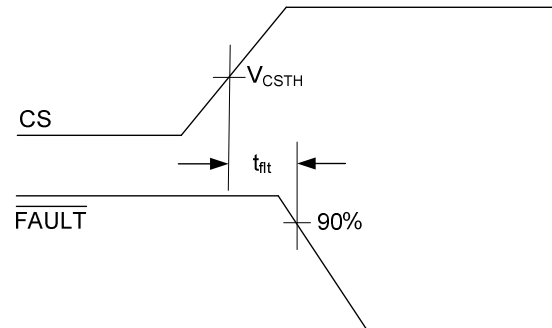


Figure 5: CS to FAULT Waveform Definitions

Parameter Temperature Trends

Figures 6-33 provide information on the experimental performance of the AUIRS212(7, 71, 8, 81)S HVIC. The line plotted in each figure is generated from actual lab data.

A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental curves. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

A different set of individual samples was used to generate curves of parameter trends vs. supply voltage.

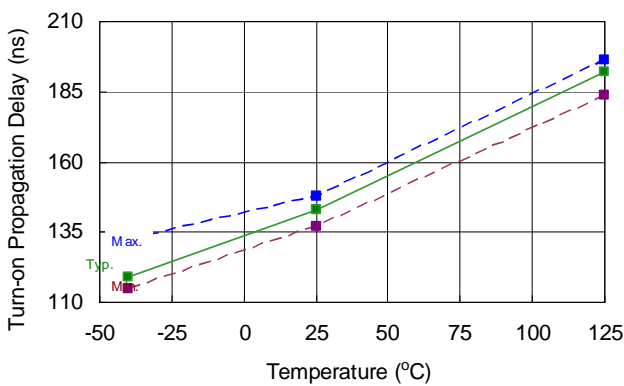


Figure 6A. Turn-On Propagation Delay vs. Temperature

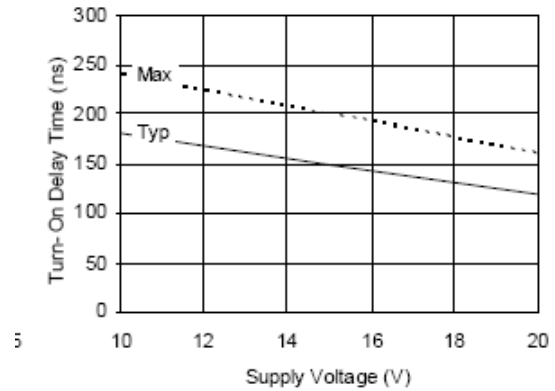


Figure 6B. Turn-On Propagation Delay vs. Supply Voltage

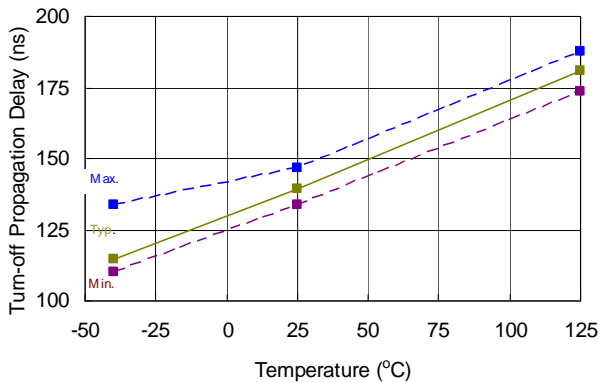


Figure 7A. Turn-Off Propagation Delay vs. Temperature

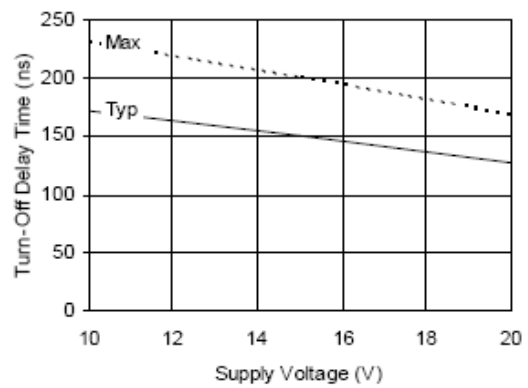


Figure 7B. Turn-Off Propagation Delay vs. Supply Voltage

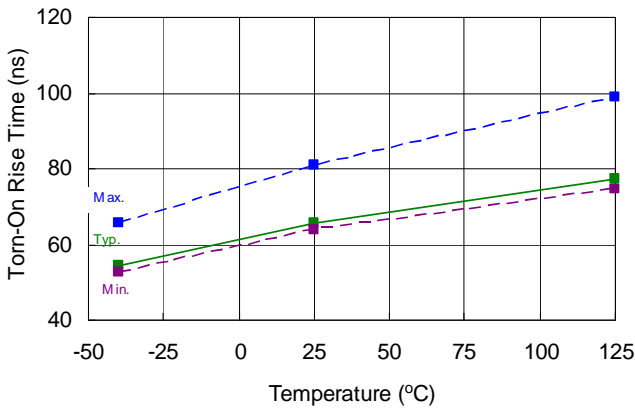


Figure 8A. Turn-On rise time vs. Temperature

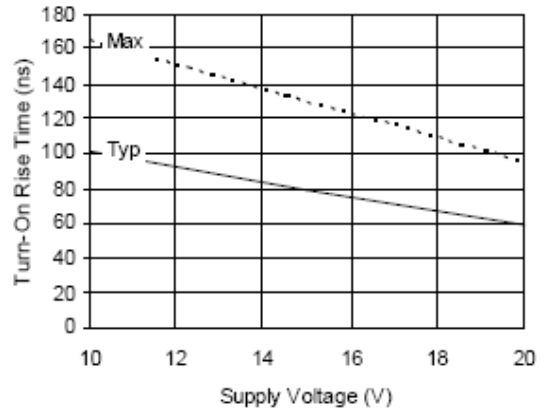


Figure 8B. Turn-On rise time vs. Voltage

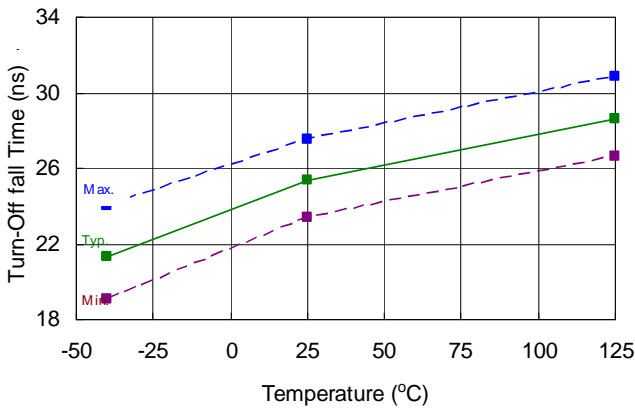


Figure 9A. Turn-Off fall time vs. Temperature

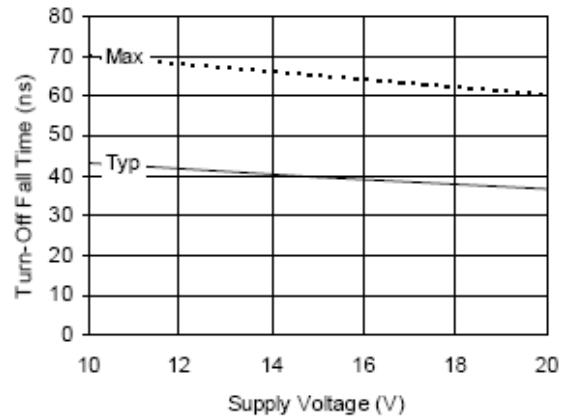


Figure 9B. Turn-Off fall time vs. Voltage

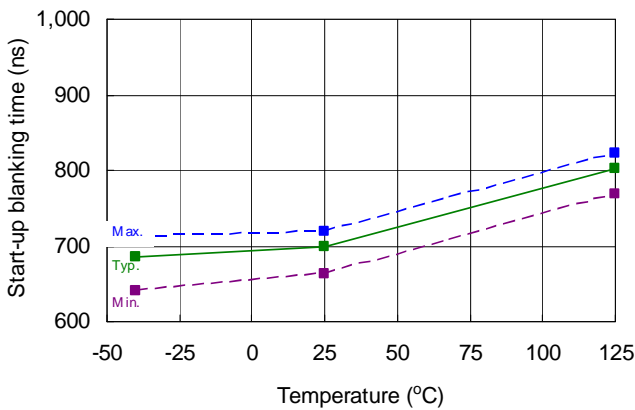


Figure 10A. Star-up blanking time vs. Temperature

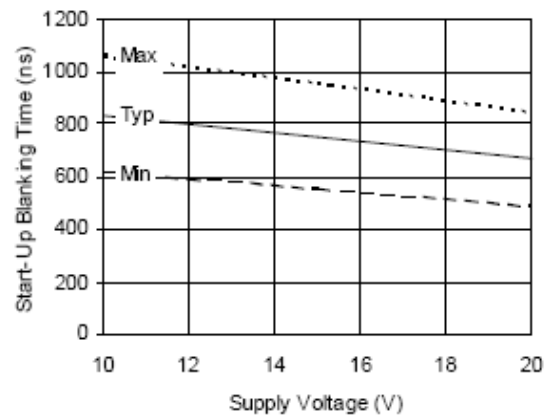


Figure 10B. Start-up blanking time vs. Voltage

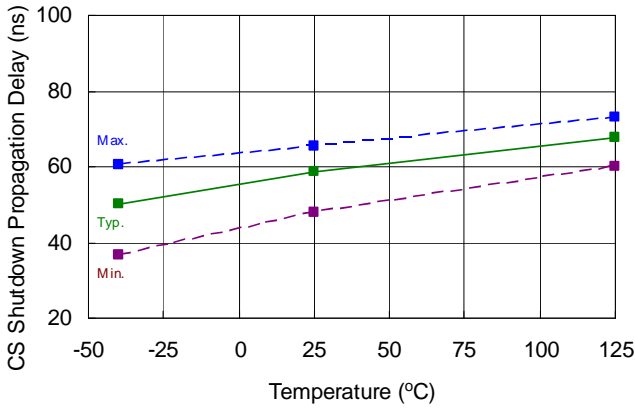


Figure 11A. CS Shutdown Prop. delay vs. Temperature

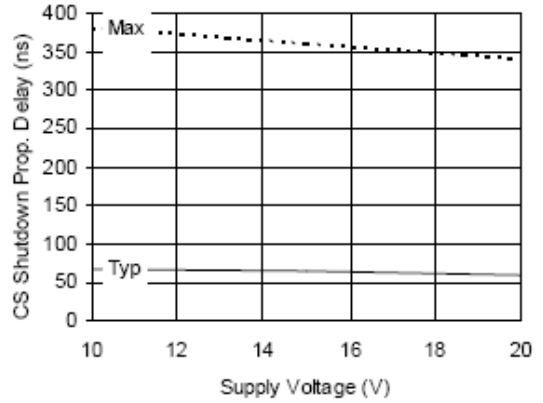


Figure 11B. CS Shutdown Prop. delay vs. Voltage

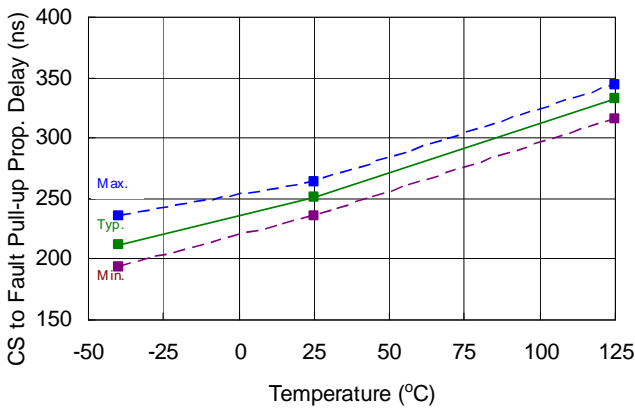


Figure 12A. CS to Fault pull-up Prop. delay vs. Temperature

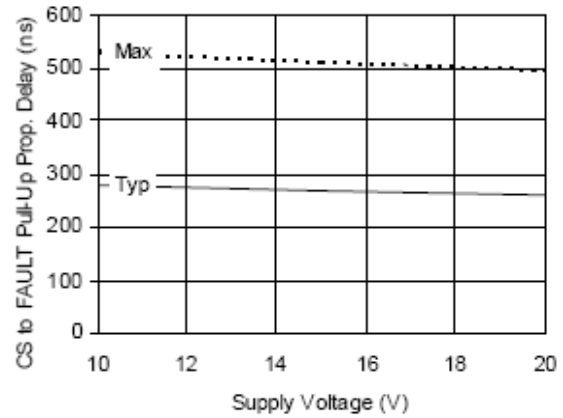


Figure 12B. CS to Fault Prop. delay vs. Voltage

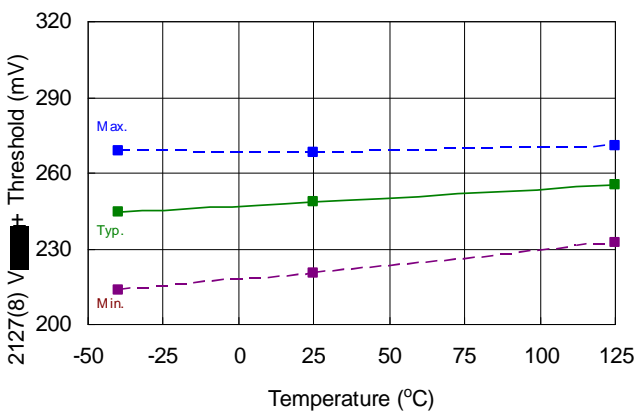


Figure 13A. 2127(8) V_{CSTH+} threshold voltage vs. Temperature

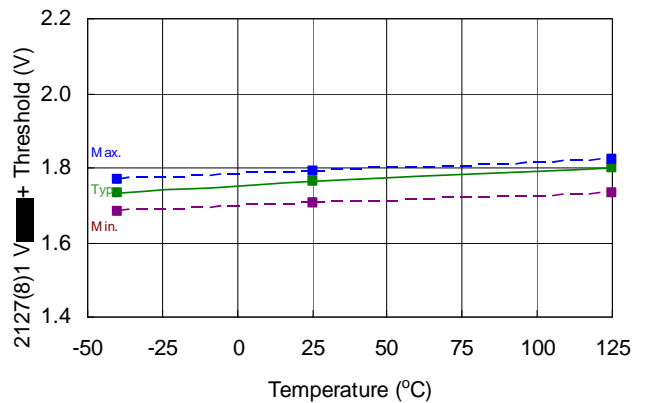


Figure 13B. 2127(8)1 V_{CSTH+} threshold voltage vs. Temperature

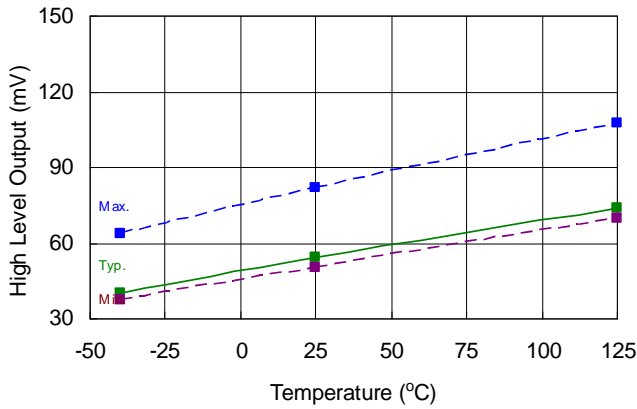


Figure 14A. High level output ($I_o = 2\text{mA}$) vs. Temperature

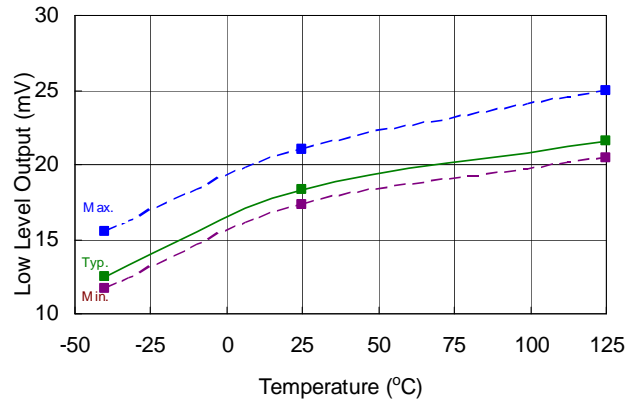


Figure 14B. Low level output ($I_o = 2\text{mA}$) vs. Temperature

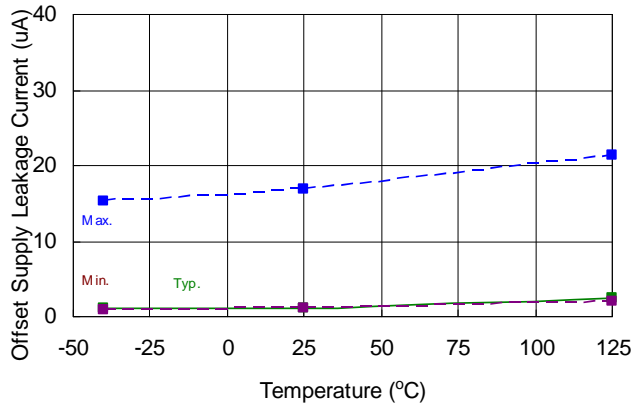


Figure 15A. Offset supply leakage current vs. Temperature

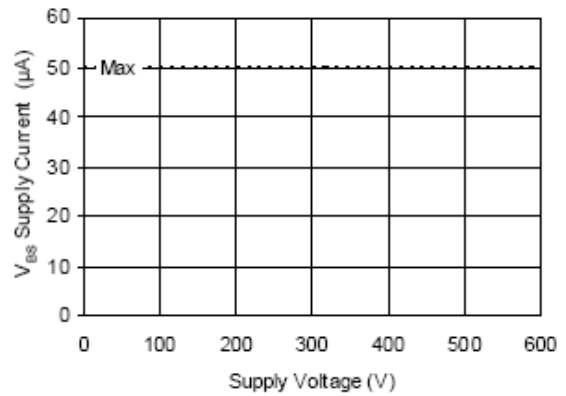


Figure 15B. High-side floating well offset supply leakage current vs. Voltage

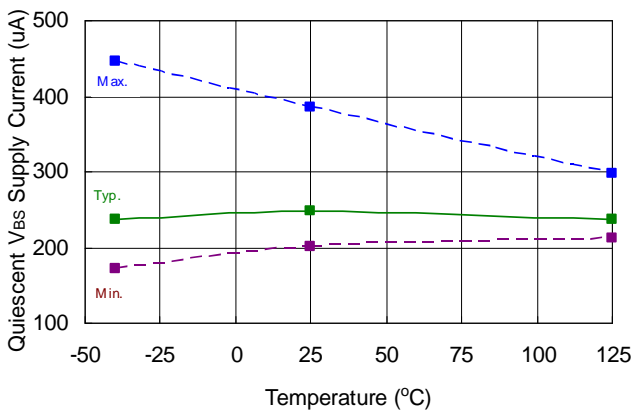


Figure 16A. V_{BS} supply current vs. Temperature

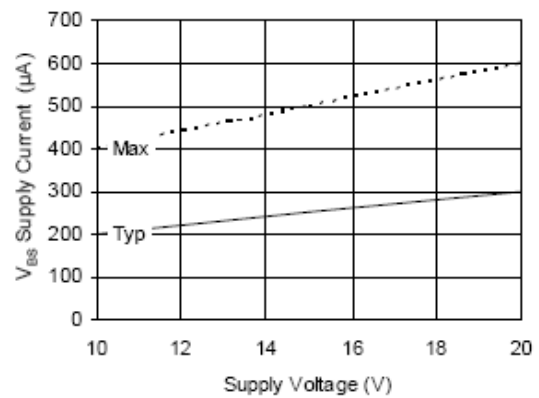


Figure 16B. V_{BS} supply current vs. Voltage

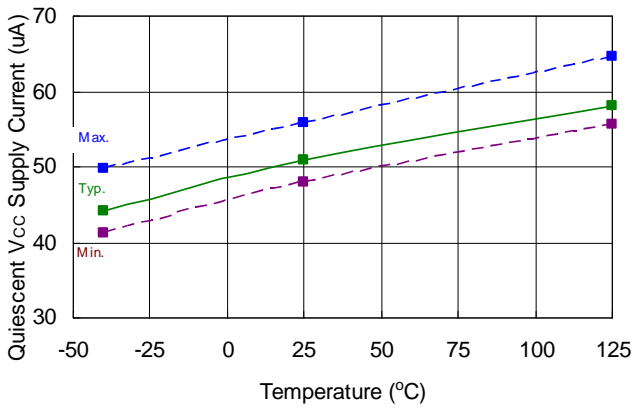


Figure 17A. V_{CC} supply current vs. Temperature

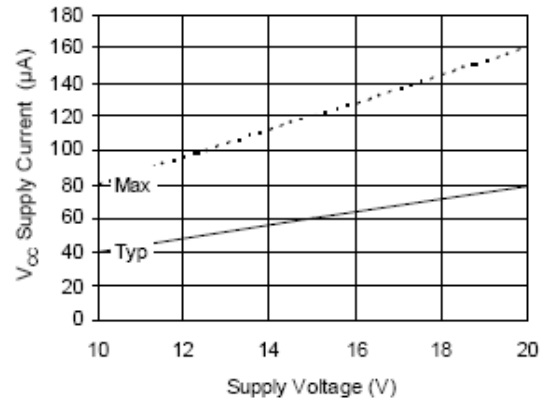


Figure 17B. V_{CC} supply current vs. Voltage

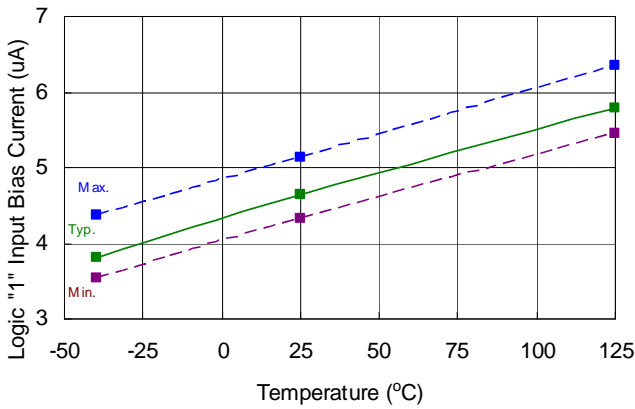


Figure 18A. Logic "1" input bias current vs. Temperature

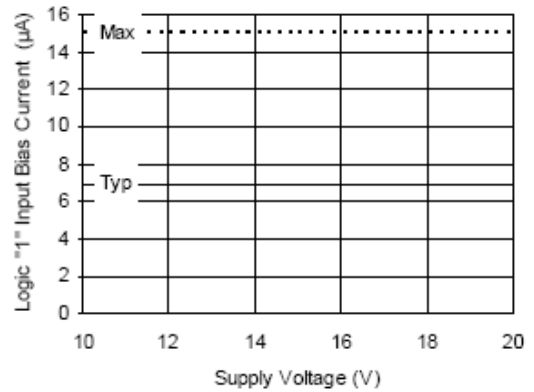


Figure 18B. Logic "1" input bias current vs. Voltage

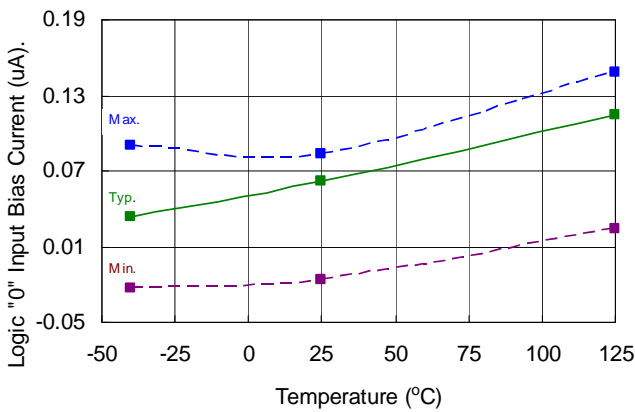


Figure 19A. Logic "0" input bias current vs. Temperature

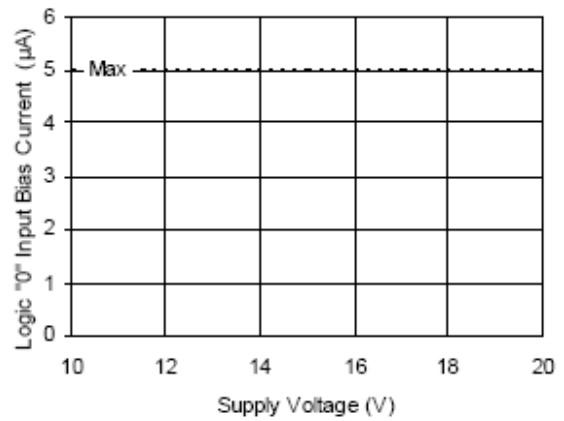


Figure 19B. Logic "0" input bias current vs. Voltage

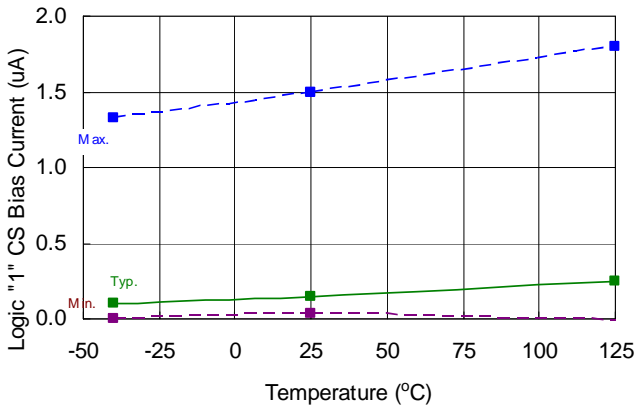


Figure 20A. Logic "1" CS bias current vs. Temperature

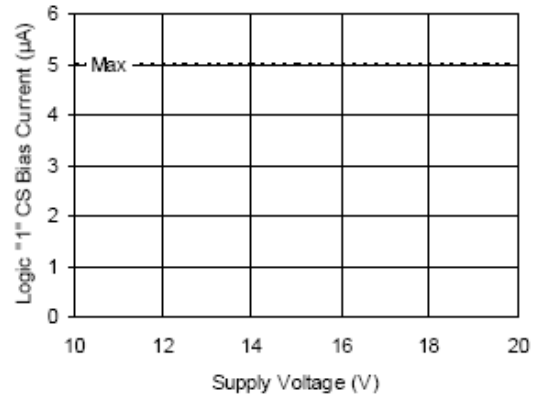


Figure 20B. Logic "1" CS bias current vs. Voltage

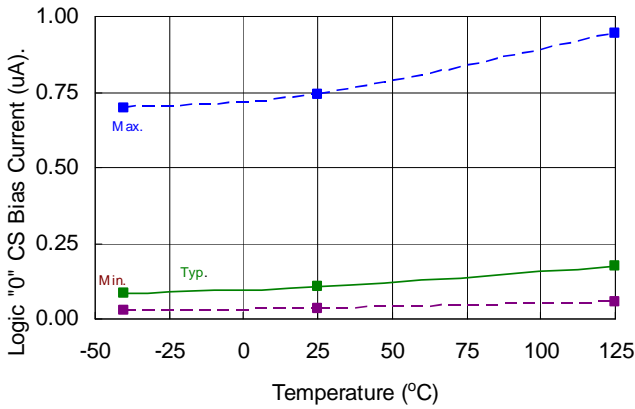


Figure 21A. Logic "0" CS bias current vs. Temperature

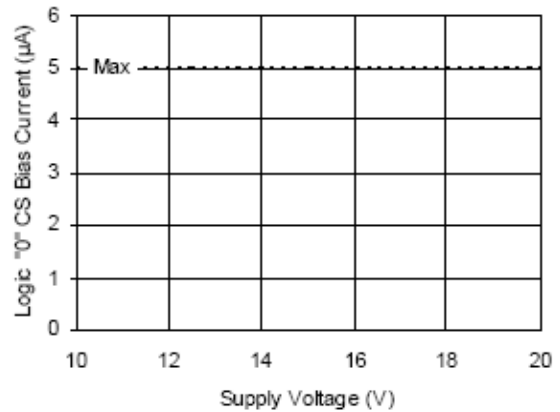


Figure 21B. Logic "0" CS bias current vs. Voltage

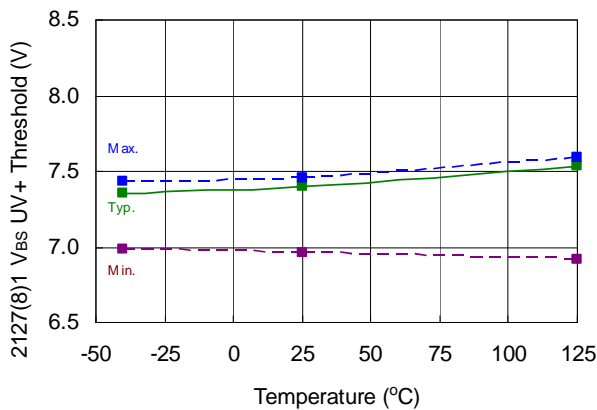


Figure 22A. 2127(8)1 V_{BS} UV threshold + vs. Temperature

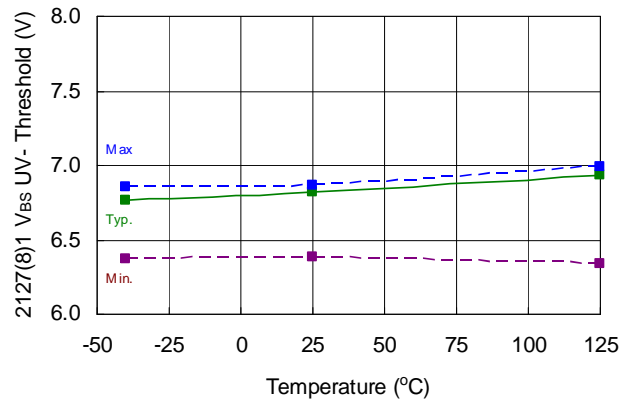


Figure 22B. 2127(8)1 V_{BS} UV threshold - vs. Temperature

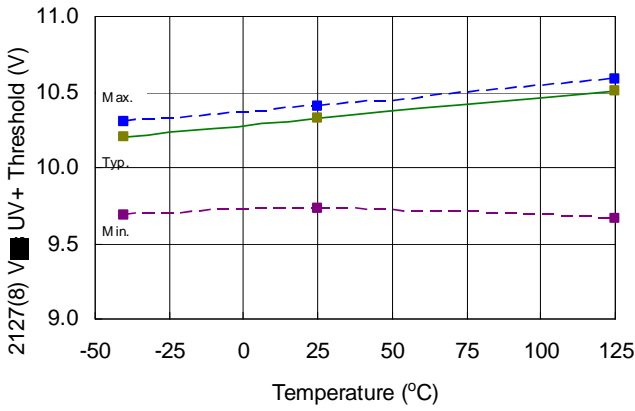


Figure 23A. 2127(8) V_{BS} UV threshold + vs. Temperature

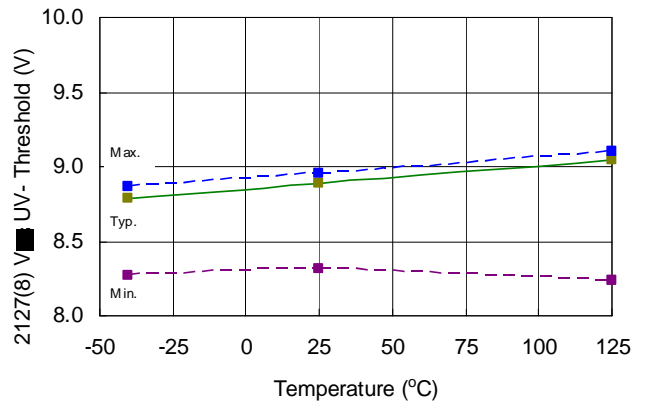


Figure 23B. 2127(8) V_{BS} UV threshold - vs. Temperature

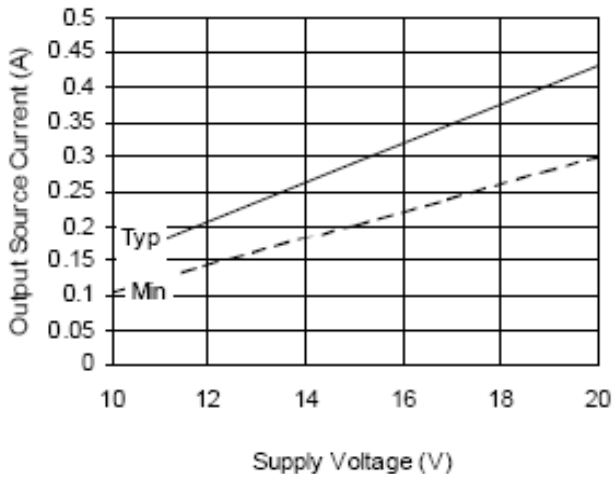


Figure 24. Output source current vs. Voltage

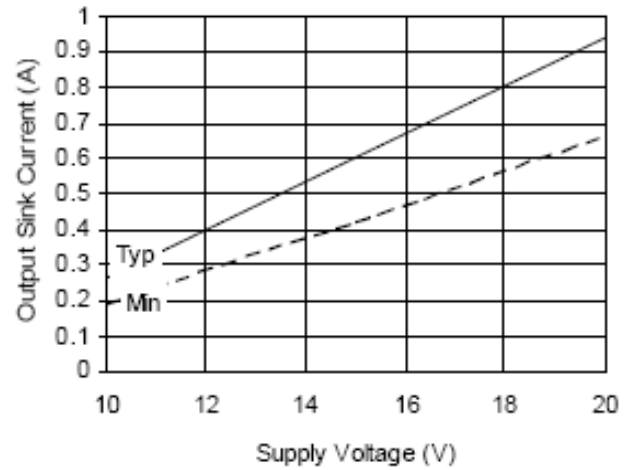
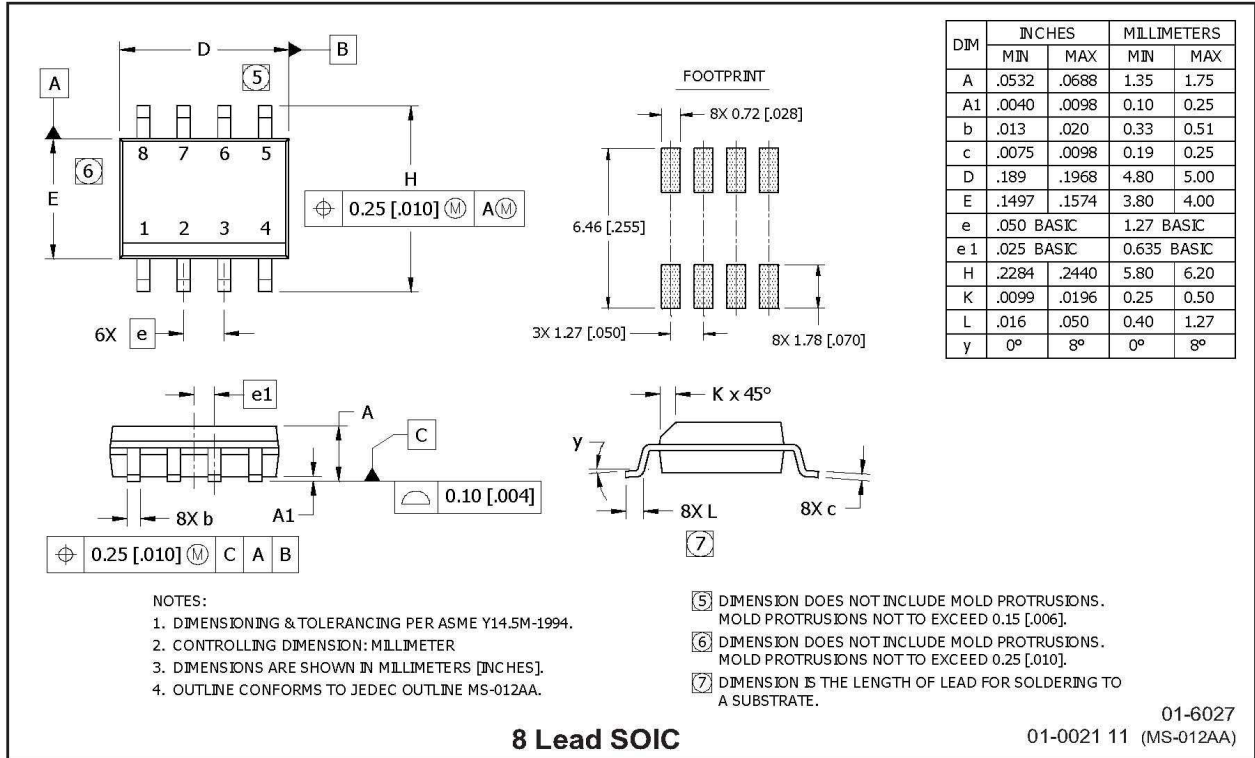
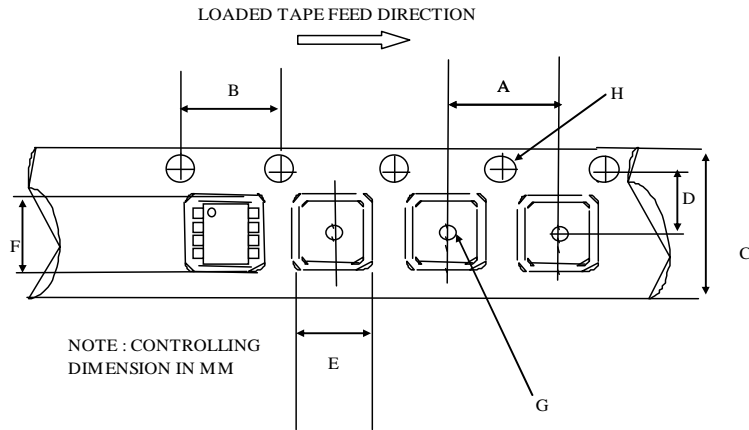


Figure 25. Output sink current vs. Voltage

Package Details: SOIC8

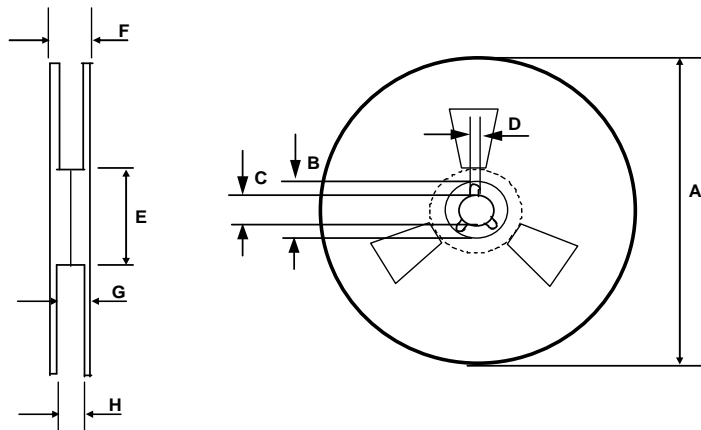


Tape and Reel Details: SOIC8



CARRIER TAPE DIMENSION FOR 8SOICN

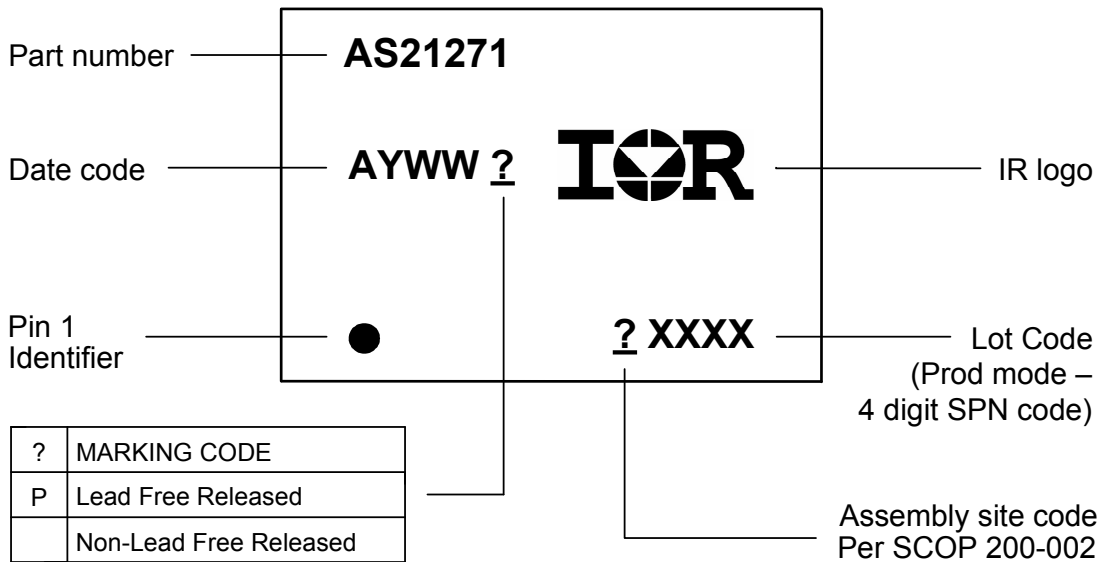
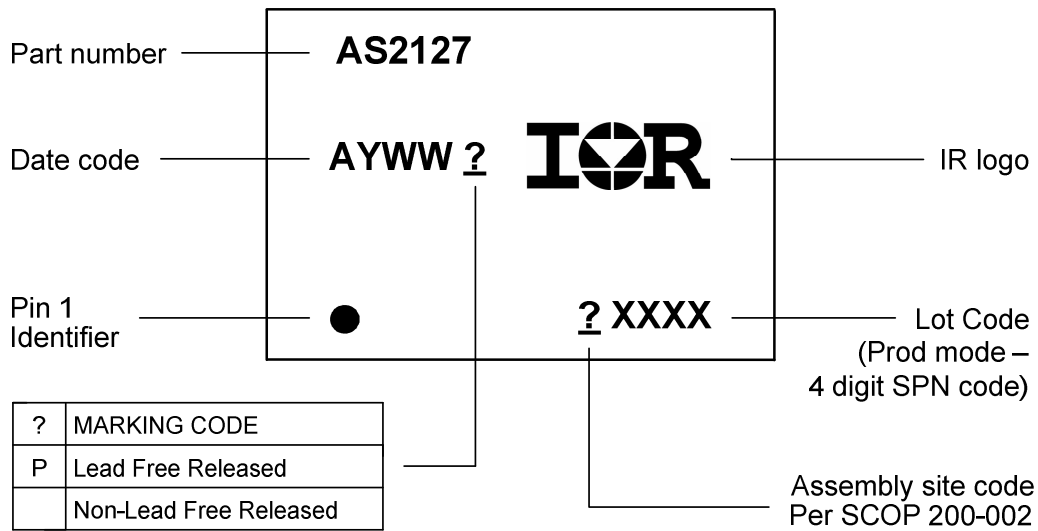
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

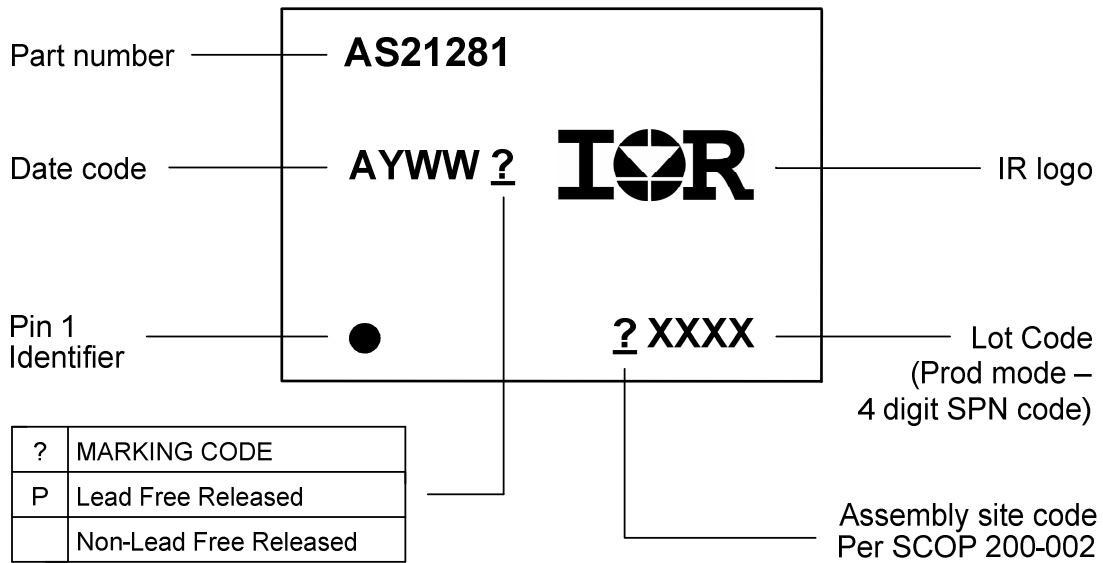
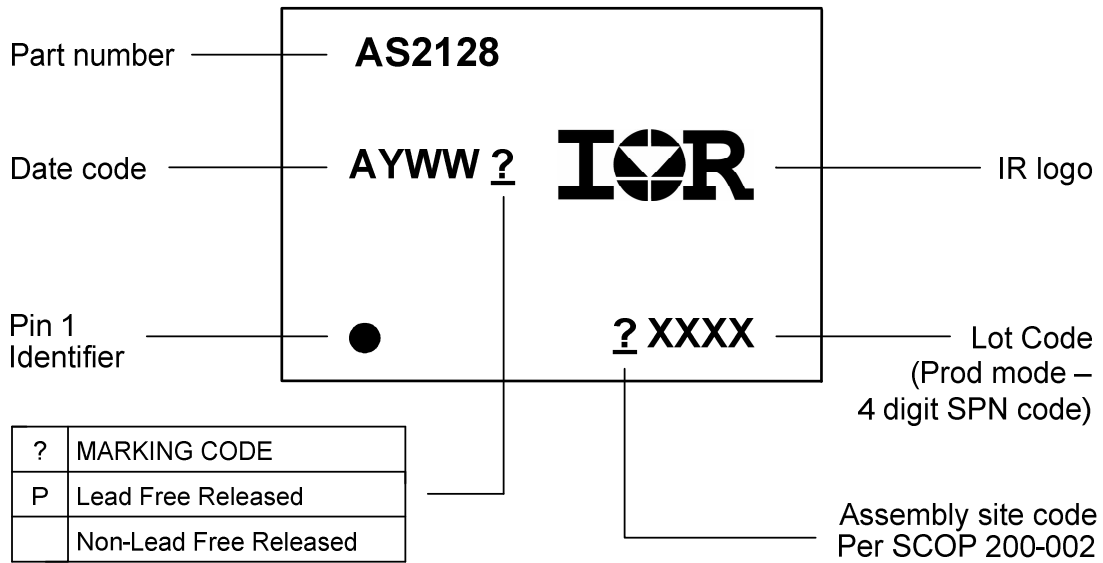


REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information





Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2127S	SOIC8	Tube/Bulk	95	AUIRS2127S
		Tape and Reel	2500	AUIRS21271STR
AUIRS21271S	SOIC8	Tube/Bulk	95	AUIRS21271S
		Tape and Reel	2500	AUIRS21271STR
AUIRS2128S	SOIC8	Tube/Bulk	95	AUIRS2128S
		Tape and Reel	2500	AUIRS2128STR
AUIRS21281S	SOIC8	Tube/Bulk	95	AUIRS21281S
		Tape and Reel	2500	AUIRS21281STR

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